(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 445 007 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
26.07.2017 Bulletin 2017/30

(21) Application number: **11185564.9**

(22) Date of filing: **18.10.2011**

(51) Int Cl.:
H01L 25/16 *(2006.01)* ***H01L 33/48*** *(2010.01)*
H01L 33/62 *(2010.01)* *H01L 33/52* *(2010.01)*
F21V 23/00 *(2015.01)* *H05K 1/02* *(2006.01)*
F21Y 115/10 *(2016.01)* *F21Y 113/13* *(2016.01)*
F21Y 105/10 *(2016.01)*

(54) Multichip package structure using a constant voltage power supply

Multichip-Verpackungsstruktur mit Konstantspannungs-Stromversorgung

Structure de boîtier à plusieurs puces utilisant une alimentation électrique à tension constante

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **22.10.2010 TW 099136124**

(43) Date of publication of application:
25.04.2012 Bulletin 2012/17

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The instant disclosure relates to a multichip package structure, and more particularly, to a multichip package structure using a constant voltage power supply.

2. Description of Related Art

[0002] The invention of the lamp greatly changed the style of building construction and the living style of human beings, allowing people to work during the night. Traditional lighting devices such as lamps that adopt incandescent bulbs, fluorescent bulbs, or power-saving bulbs have been generally well-developed and used intensively indoor illumination. However, compared to the newly developed light-emitting-diode (LED) lamps, these traditional lamps have the disadvantages of quick attenuation, high power consumption, high heat generation, short working life, high fragility, and being not recyclable. Thus, various LED package structures are created to replace the traditional lighting devices. JP06077540 discloses a multichip package structure with light emitting chips arranged on a region on a substrate and surrounded by a thick reflecting frame. A thinner frame is formed between light emitting chips within the region for increasing visibility. The LED chips may be covered by a transparent resin member. An integrated circuit chip is also arranged on the same substrate.

[0003] JP2009117080 discloses an illumination device equipped with a plurality of light sources with different emission colors, capable of easily changing luminance and/or color temperature by adjusting the emission intensity of each of the plurality of light sources.

[0004] WO2008/002073 relates to an artificial solar light system using light emitting diodes arranged in modules with different color temperatures.

[0005] JP2009231027 discloses an illumination device with groups of LEDs of different colors arranged on a substrate and separated by partitions of resin or metal. Each group of LEDs is covered by a translucent sealing member comprising fluorescent material.

SUMMARY OF THE INVENTION

[0006] The invention is defined in claim 1. Embodiments of the invention are set out in the dependent claims. Examples not falling under the terms of the definition of claim 1 do not form part of the present invention even though they may be referred to as "embodiments" in the description. They are merely examples useful for understanding the present invention.

[0007] One particular aspect of the instant disclosure is to provide a multichip package structure that can use a constant voltage power supply as power supply source.

[0008] To achieve the above-mentioned advantages, one embodiment of the instant disclosure provides a multichip package structure, comprising: a substrate unit, a light-emitting unit, a current-limiting unit, a frame unit and a package unit. The substrate unit includes a substrate body having a first chip-placing region and a second chip-placing region formed on the top surface of the substrate body. The light-emitting unit includes a plurality of light-emitting chips electrically connected to and disposed on the first chip-placing region. The current-limiting unit includes at least one current-limiting chip electrically connected to and disposed on the second chip-placing region, and the current-limiting chip is electrically connected to the light-emitting unit. The frame unit includes a first surrounding colloid frame and a second surrounding colloid frame surroundingly formed on the top surface of the substrate body. The first surrounding colloid frame surrounds the light-emitting chips to form a first colloid position limiting space corresponding to the first chip-placing region, and the second surrounding colloid frame surrounds the current-limiting chip to form a second colloid position limiting space corresponding to the second chip-placing region. The package unit includes a first package colloid body filled into the first colloid position limiting space to cover the light-emitting chips and a second package colloid body filled into the second colloid position limiting space to cover the current-limiting chip.

[0009] Therefore, the light-emitting chips and the at least one current-limiting chip are electrically connected to the same substrate body, thus the multichip package structure can use the constant voltage power supply as power supply source.

[0010] To further understand the techniques, means and effects the instant disclosure takes for achieving the prescribed objectives, the following detailed descriptions and appended drawings are hereby referred, such that, through which, the purposes, features and aspects of the instant disclosure can be thoroughly and concretely appreciated. However, the appended drawings are provided solely for reference and illustration, without any intention that they be used for limiting the instant disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

FIG. 1A shows a perspective, schematic view of the multichip package structure according to the first embodiment of the instant disclosure;

FIG. 1B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the first embodiment of the instant disclosure;

FIG. 1C shows a top, schematic view of the multichip package structure according to the first embodiment of the instant disclosure;

FIG. 1D shows a function block diagram of the multichip package structure according to the first em-

bodiment of the instant disclosure;
FIG. 2A shows a top, schematic view of the multichip package structure according to the second embodiment of the instant disclosure;
FIG. 2B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the second embodiment of the instant disclosure;
FIG. 3 shows a top, schematic view of the multichip package structure according to the third embodiment of the instant disclosure;
FIG. 4A shows a top, schematic view of the multichip package structure according to the fourth embodiment of the instant disclosure;
FIG. 4B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the fourth embodiment of the instant disclosure;
FIG. 5A shows a top, schematic view of the multichip package structure according to the fifth embodiment of the instant disclosure;
FIG. 5B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the fifth embodiment of the instant disclosure;
FIG. 6A shows a top, schematic view of the multichip package structure according to the sixth embodiment of the instant disclosure;
FIG. 6B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the sixth embodiment of the instant disclosure;
FIG. 7A shows a top, schematic view of the multichip package structure according to the seventh embodiment of the instant disclosure;
FIG. 7B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the seventh embodiment of the instant disclosure;
FIG. 8 shows a top, schematic view of the multichip package structure according to the eighth embodiment of the instant disclosure;
FIG. 9A shows a top, schematic view of the multichip package structure according to the ninth embodiment of the instant disclosure;
FIG. 9B shows a lateral, cross-sectional, schematic view of the multichip package structure according to the ninth embodiment of the instant disclosure;
FIG. 10 shows a lateral, cross-sectional, schematic view of the multichip package structure according to the tenth embodiment of the instant disclosure; and
FIG. 11 shows a partial, top, schematic view of the substrate unit using standby pads.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] Referring to FIGS. 1A to 1D, the first embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply S. The multichip package structure Z comprises a substrate unit 1, a light-emitting unit 2, a current-limiting unit C, a frame unit 3 and a package unit 4.

[0013] The substrate unit 1 includes a substrate body 10 having a first chip-placing region 11 and a second chip-placing region 12 formed on the top surface of the substrate body 10. For example, the substrate body 10 includes a circuit substrate 100, a heat-dissipating layer 101 disposed on the bottom surface of the circuit substrate 100, a plurality conductive pads 102 disposed on the top surface of the circuit substrate 100, and an insulative layer 103 disposed on the top surface of the circuit substrate 100 to expose the conductive pads 102. Hence, the heat-dissipating efficiency of the circuit substrate 100 is increased by using the heat-dissipating layer 101, and the insulative layer 103 is a solder mask for only exposing the conductive pads 102 in order to achieve local soldering. However, the above-mentioned definition of the substrate body 10 is not to limit the instant disclosure, for example, the substrate body 10 can be a PCB (Printed Circuit Board), a flexible substrate, an aluminum substrate, a ceramic substrate, or a copper substrate.

[0014] The light-emitting unit 2 includes a plurality of light-emitting chips (bare die state) 20 electrically connected to and disposed on the first chip-placing region 11. For example, each light-emitting chip 20 may be an LED (Light-emitting diode) such as a blue LED, and each light-emitting chip 20 can be electrically connected to the first chip-placing region 11 by wire bonding. In other words, designer can plan a predetermined first chip-placing region 11 on the substrate body 10 in advance, thus the first light-emitting chips 20 can be placed on the first chip-placing region 11.

[0015] The current-limiting unit C includes at least one current-limiting chip C1 electrically connected to and disposed on the second chip-placing region 12, and the current-limiting chip C1 is electrically connected to the light-emitting unit 2. Of course, the current-limiting unit C can also include a plurality of current-limiting chips C1 on the second chip-placing region 12 for different requirements of amperage or current. For example, the current-limiting chip C1 can be electrically connected to the second chip-placing region 12 by wire bonding and electrically connected between the constant voltage power supply S and the light-emitting unit 2 (as shown in FIG. 1D). In other words, designer can plan a predetermined second chip-placing region 12 on the substrate body 10 in advance, thus the current-limiting chip C1 can be placed on the second chip-placing region 12. In addition, the current-limiting chip C1 is electrically connected between the constant voltage power supply S and the light-emitting unit 2, thus the light-emitting unit 2 can obtain constant voltage from the constant voltage power supply S through the current-limiting chip C1. Moreover, the instant disclosure further comprises a control unit 5 that includes at least one PWM (Pulse Width Modulation) control module 50 selectively electrically connected to the current-limiting chip C1, thus the current-limiting unit C can be electrically connected between the control unit 5 and the light-emitting unit 2. Of course, the control unit 5 also can be omitted from the instant disclosure. For example, when

the control unit 5 is electrically connected between the constant voltage power supply S and the current-limiting unit C, the PWM control module 50 can control the light-emitting chip 20 to generate a predetermined pulse frequency, such as 50Hz, 60Hz, ..., 120Hz, etc.

[0016] The frame unit 3 includes a first surrounding colloid frame 30 and a second surrounding colloid frame 31 surroundingly formed on the top surface of the substrate body 10 by coating or other forming method. The first surrounding colloid frame 30 surrounds the light-emitting chips 20 to form a first colloid position limiting space 300 corresponding to the first chip-placing region 11, and the second surrounding colloid frame 31 surrounds the current-limiting chip C1 to form a second colloid position limiting space 310 corresponding to the second chip-placing region 12. The first surrounding colloid frame 30 and the second surrounding colloid frame 31 are separated from each other by a predetermined distance.

[0017] For example, the method for forming the first surrounding colloid frame 30 (or the second surrounding colloid frame 31) includes: first, surroundingly coating liquid colloid (not shown) on the top surface of the substrate body 10. In addition, the liquid colloid can be coated on the substrate body 10 to form any shapes according to different requirements (such as a circular shape, a square or a rectangular shape etc.). The thixotropic index of the liquid colloid may be between 4 and 6, the pressure of coating the liquid colloid on the top surface of the substrate body 10 may be between 350 kpa and 450 kpa, and the velocity of coating the liquid colloid on the top surface of the substrate body 10 may be between 5 mm/s and 15 mm/s. The liquid colloid is surroundingly coated on the top surface of the substrate body 10 from a start point to a termination point, and the position of the start point and the position of the termination point are substantially the same, thus the first surrounding colloid frame 30 (or the second surrounding colloid frame 31) has a micro convex portion close to the start point and the termination point. Furthermore, the method further includes: hardening or curing the liquid colloid to form a first surrounding colloid frame 30. In addition, the liquid colloid is hardened by baking, the baking temperature may be between 120°C and 140°C, and the baking time may be between 20 minute and 40 minute. Therefore, the first surrounding colloid frame 30 has an arc shape formed on the top surface thereof, the first surrounding colloid frame 30 has a radius tangent T and the angle θ of the radius tangent T relative to the top surface of the substrate body 10 may be between 40° and 50°, the maximum height H of the first surrounding colloid frame 30 relative to the top surface of the substrate body 10 may be between 0.3 mm and 0.7 mm, the width D of the bottom side of the first surrounding colloid frame 30 may be between 1.5 mm and 3 mm, the thixotropic index of the first surrounding colloid frame 30 may be between 4 and 6, and the first surrounding colloid frame 30 is formed by mixing inorganic additive with white thermohardening colloid.

[0018] The package unit 4 includes a first package colloid body 40 filled into the first colloid position limiting space 300 to cover the light-emitting chips 20 and a second package colloid body 41 filled into the second colloid position limiting space 310 to cover the current-limiting chip C1. The first package colloid body 40 and the second package colloid body 41 are separated from each other by a predetermined distance, and the first surrounding colloid frame 30 and the second package colloid body 41 are separated from each other by a predetermined distance. For example, the first package colloid body 40 may be a light-permitting colloid body such as cured phosphor colloid or cured transparent colloid, thus blue light beams L1 generated by the light-emitting chips 20 (the blue LED chips) can pass through the first package colloid body 40 (the cured phosphor colloid) to generate white light beams L2 that are similar to the light source generate by sun lamp. In addition, the second package colloid body 41 may be a cured opaque colloid covering the current-limiting chip C1, thus the second package colloid body 41 can prevent the current-limiting chip C1 from being damaged or affected by lighting of the white light beams L2.

[0019] The substrate unit 1 further includes at least one heat-insulating slot 13 passing through the substrate body 10, and the heat-insulating slot 13 is formed between the light-emitting unit 2 and the current-limiting unit C or between the first surrounding colloid frame 30 and the second surrounding colloid frame 31. Hence, the heat-transmitting path between the light-emitting unit 2 and the current-limiting unit C can be effectively reduced by using the heat-insulating slot 13, thus the velocity of transmitting the heat generated by the current-limiting chip C1 to the light-emitting unit 2 can be effectively decreased.

[0020] Referring to FIGS. 2A and 2B, the second embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 2A with FIG. 1A (or FIG. 2B with FIG. 1B), the difference between the second embodiment and the first embodiment is that: the heat-insulating slot 13 shown in FIG. 2A can be omitted in the second embodiment. For example, when the heat generated by the current-limiting chip C1 is very small, the user can use the second embodiment.

[0021] Referring to FIG. 3, the third embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 3 with FIG. 1C, the difference between the third embodiment and the first embodiment is that: the current-limiting unit C is disposed between the first surrounding colloid frame 30 and the second surrounding colloid frame 31, the second surrounding colloid frame 31 surrounds the first surrounding colloid frame 30, the second package colloid body 41 surrounds the first package colloid body 40, and the first surrounding colloid frame 30 is connected with the second package colloid

body 41. In other words, the first surrounding colloid frame 30 only surrounds the light-emitting chips 20, the second surrounding colloid frame 31 simultaneously surrounds the light-emitting chips 20, the first surrounding colloid frame 30 and the current-limiting chip C1, thus the first surrounding colloid frame 30 and the second surrounding colloid frame 31 are arranged to form a concentric circle.

[0022] The substrate unit 1 further includes at least one heat-insulating slot 13 passing through the substrate body 10, and the heat-insulating slot 13 is formed between the light-emitting unit 2 and the current-limiting unit C or between the first surrounding colloid frame 30 and the second surrounding colloid frame 31. Hence, the heat-transmitting path between the light-emitting unit 2 and the current-limiting unit C can be effectively reduced by using the heat-insulating slot 13, thus the velocity of transmitting the heat generated by the current-limiting chip C1 to the light-emitting unit 2 can be effectively decreased. Of course, when the heat generated by the current-limiting chip C1 is very small, the heat-insulating slot 13 shown in FIG. 3 can be omitted.

[0023] Referring to FIGS. 4A and 4B, the fourth embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). The multichip package structure Z comprises a substrate unit 1, a light-emitting unit 2, a current-limiting unit C, a frame unit 3 and a package unit 4.

[0024] The substrate unit 1 includes a substrate body 10 having two first chip-placing regions 11 and a second chip-placing region 12 formed on the top surface of the substrate body 10. For example, the substrate body 10 includes a circuit substrate 100, a heat-dissipating layer 101 disposed on the bottom surface of the circuit substrate 100, a plurality conductive pads 102 disposed on the top surface of the circuit substrate 100, and an insulative layer 103 disposed on the top surface of the circuit substrate 100 to expose the conductive pads 102.

[0025] The light-emitting unit 2 includes at least one first light-emitting module 2a for generating first color temperature and at least one second light-emitting module 2b for generating second color temperature. The first light-emitting module 2a includes a plurality of first light-emitting chips 20a electrically connected to and disposed on one of the first chip-placing regions 11, and the second light-emitting module 2b includes a plurality of second light-emitting chips 20b electrically connected to and disposed on the other first chip-placing region 11. For example, each first light-emitting chip 20a and each second light-emitting chip 20b may be a blue LED, and each first light-emitting chip 20a and each second light-emitting chip 20b can be respectively and electrically connected to the two first chip-placing regions 11 by wire bonding.

[0026] The current-limiting unit C includes at least one current-limiting chip C1 electrically connected to and disposed on the second chip-placing region 12, and the current-limiting chip C1 is electrically connected to the light-emitting unit 2. Of course, the current-limiting unit C can also include a plurality of current-limiting chips C1 on the second chip-placing region 12 for different requirements of amperage or current. For example, the current-limiting chip C1 can be electrically connected to the second chip-placing region 12 by wire bonding and electrically connected between the constant voltage power supply (not shown) and the light-emitting unit 2. In addition, the current-limiting chip C1 is electrically connected between the constant voltage power supply (not shown) and the light-emitting unit 2, thus the light-emitting unit 2 can obtain constant voltage from the constant voltage power supply (not shown) through the current-limiting chip C1.

[0027] The frame unit 3 includes two first surrounding colloid frames 30 and a second surrounding colloid frame 31 surroundingly formed on the top surface of the substrate body 10 by coating or other forming method. The two first surrounding colloid frames 30 respectively surround the first light-emitting module 2a and the second light-emitting module 2b to respectively form two first colloid position limiting spaces 300 corresponding to the two first chip-placing regions 11, and the second surrounding colloid frame 31 surrounds the current-limiting chip C1 to form a second colloid position limiting space 310 corresponding to the second chip-placing region 12. The two first surrounding colloid frames 30 are separated from each other and arranged on the substrate body 10 in parallel, and each first surrounding colloid frame 30 and the second surrounding colloid frame 31 are separated from each other.

[0028] The package unit 4 includes two first package colloid bodies (40a, 40b) and a second package colloid body 41. The two first package colloid bodies (40a, 40b) are respectively filled into the two first colloid position limiting spaces 300 to respectively cover the first light-emitting module 2a and the second light-emitting module 2b, and the second package colloid body 41 is filled into the second colloid position limiting space 310 to cover the current-limiting chip C1. Each first package colloid bodies (40a, 40b) and the second package colloid body 41 are separated from each other, and each first surrounding colloid frame 30 and the second package colloid body 41 are separated from each other. For example, one first package colloid body 40a may be a cured phosphor colloid with first color, the other first package colloid body 40b may be a cured phosphor colloid with second color, and the second package colloid body 41 may be a cured opaque colloid.

[0029] The substrate unit 1 further includes at least one heat-insulating slot 13 passing through the substrate body 10, and the heat-insulating slot 13 is formed between the light-emitting unit 2 and the current-limiting unit C or between one of the two first surrounding colloid frames 30 and the second surrounding colloid frame 31, thus the velocity of transmitting the heat generated by the current-limiting chip C1 to the light-emitting unit 2 can be effectively decreased. Of course, when the heat generated by the current-limiting chip C1 is very small, the heat-insulating slot 13 can be omitted.

[0030] The first light-emitting structure N1 may comprises the substrate body 10, the first light-emitting chips 20a, one first surrounding colloid frame 30 and one first package colloid body 40a. The second light-emitting structure N2 may comprises the substrate body 10, the second light-emitting chips 20b, the other first surrounding colloid frame 30 and the other first package colloid body 40b.

[0031] Referring to FIGS. 5A and 5B, the fifth embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 5A with FIG. 4A (or FIG. 5B with FIG. 4B), the difference between the fifth embodiment and the fourth embodiment is that: in the fifth embodiment, the two first surrounding colloid frames 30 can be arranged on the substrate body 10 in series.

[0032] Referring to FIGS. 6A and 6B, the sixth embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 6A with FIG. 5A (or FIG. 6B with FIG. 5B), the difference between the sixth embodiment and the fifth embodiment is that: in the sixth embodiment, each first surrounding colloid frame 30 may be a cured phosphor colloid. In other words, phosphor powders can be selectively add to each first surrounding colloid frame 30 according to different requirements, thus dark bands generated between the two first package colloid bodies (40a, 40b) can be effectively decreased or eliminated.

[0033] Referring to FIGS. 7A and 7B, the seventh embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). The multichip package structure Z comprises a substrate unit 1, a light-emitting unit 2, a current-limiting unit C, a frame unit 3 and a package unit 4.

[0034] The substrate unit 1 includes a substrate body 10 having two first chip-placing regions 11 and a second chip-placing region 12 formed on the top surface of the substrate body 10. The light-emitting unit 2 includes at least one first light-emitting module 2a for generating first color temperature and at least one second light-emitting module 2b for generating second color temperature. The first light-emitting module 2a includes a plurality of first light-emitting chips 20a electrically connected to and disposed on one of the first chip-placing regions 11, and the second light-emitting module 2b includes a plurality of second light-emitting chips 20b electrically connected to and disposed on the other first chip-placing region 11. The current-limiting unit C includes at least one current-limiting chip C1 electrically connected to and disposed on the second chip-placing region 12, and the current-limiting chip C1 is electrically connected to the light-emitting unit 2.

[0035] The frame unit 3 includes two first surrounding colloid frames (30a, 30b) and a second surrounding colloid frame 31 surroundingly formed on the top surface of the substrate body 10 by coating or other forming method. One first surrounding colloid frame 30b surrounds the other first surrounding colloid frame 30a, thus the two first surrounding colloid frames (30a, 30b) are arranged to form a concentric circle. The two first surrounding colloid frames (30a, 30b) respectively surround the first light-emitting module 2a and the second light-emitting module 2b to respectively form two first colloid position limiting spaces 300 corresponding to the two first chip-placing regions 11, the second light-emitting module 2b is disposed between the two first surrounding colloid frames (30a, 30b), and the second surrounding colloid frame 31 surrounds the current-limiting chip C1 to form a second colloid position limiting space 310 corresponding to the second chip-placing region 12. The package unit 4 includes two first package colloid bodies (40a, 40b) and a second package colloid body 41. The two first package colloid bodies (40a, 40b) are respectively filled into the two first colloid position limiting spaces 300 to respectively cover the first light-emitting module 2a and the second light-emitting module 2b, and the second package colloid body 41 is filled into the second colloid position limiting space 310 to cover the current-limiting chip C1.

[0036] The substrate unit 1 further includes at least one heat-insulating slot 13 passing through the substrate body 10, and the heat-insulating slot 13 is formed between the light-emitting unit 2 and the current-limiting unit C or between one of the two first surrounding colloid frames 30b and the second surrounding colloid frame 31, thus the velocity of transmitting the heat generated by the current-limiting chip C1 to the light-emitting unit 2 can be effectively decreased. Of course, when the heat generated by the current-limiting chip C1 is very small, the heat-insulating slot 13 can be omitted.

[0037] The first light-emitting structure N1 may comprises the substrate body 10, the first light-emitting chips 20a, one first surrounding colloid frame 30a and one first package colloid body 40a. The second light-emitting structure N2 may comprises the substrate body 10, the second light-emitting chips 20b, the other first surrounding colloid frame 30b and the other first package colloid body 40b. In addition, the second light-emitting structure N2 with high color temperature can be an outer ring to surround the first light-emitting structure N1 with low color temperature.

[0038] Referring to FIG. 8, the eighth embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 8 with FIG. 7A, the difference between the eighth embodiment and the seventh embodiment is that: in the eighth embodiment, the first light-emitting structure N1 with low color temperature can be an outer ring to surround the second light-emitting structure N2 with high color temperature.

[0039] Referring to FIGS. 9A and 9B, the ninth embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 9A with FIG. 7A (or FIG. 9B with FIG. 7B), the difference between the ninth embodiment and the seventh embodiment is that: in the ninth

embodiment, each first surrounding colloid frame (30a, 30b) may be a cured phosphor colloid. In other words, phosphor powders can be selectively add to each first surrounding colloid frame (30a, 30b) according to different requirements, thus dark bands generated between the two first package colloid bodies (40a, 40b) can be effectively decreased or eliminated.

[0040] Referring to FIG. 10, the tenth embodiment of the instant disclosure provides a multichip package structure Z using a constant voltage power supply (not shown). Comparing FIG. 10 with FIG. 7B, the difference between the tenth embodiment and the seventh embodiment is that: in the tenth embodiment, the inner first surrounding colloid frame 30a may be a cured phosphor colloid and the outer first surrounding colloid frame 30b may be a cured light-reflecting colloid. In other words, phosphor powders can be selectively add to the inner first surrounding colloid frame 30a according to different requirements, thus light beams generated by the light-emitting unit 2 can be transmitted into the inner first surrounding colloid frame 30a for effectively decreasing or eliminating dark bands generated between the two first package colloid bodies (40a, 40b). In addition, light beams generated by the light-emitting unit 2 can be effectively reflected or condensed by the outer first surrounding colloid frame 30b.

[0041] Referring to FIG. 11, in the first to the tenth embodiments, the substrate unit 1 includes a plurality of positive pads P and negative pads N disposed on the top surface of the substrate body 10. Each light-emitting chip (20 or 20a, 20b) has a positive electrode 201 and a negative electrode 202. The positive electrode 201 of each light-emitting chip 20 corresponds to at least two of the positive pads P, and the negative electrode 202 of each light-emitting chip 20 corresponds to at least two of the negative pads N. In addition, the multichip package structure further comprises a conductive wire unit W including a plurality of conductive wires W1. Every two conductive wires W1 are respectively electrically connected between the positive electrode 201 of each light-emitting chip 20 and one of the at least two positive pads P and between the negative electrode 202 of each light-emitting chip 20 and one of the at least two negative pads N. Hence, the positive electrode 201 of each light-emitting chip 20 has at least one standby positive pad P and the negative electrode 202 of each light-emitting chip 20 has at least one standby negative pad N.

[0042] When a first end of the conductive wire W1 does not correctly connect with first one of the at least two positive pads P or the at least two negative pads N (it means that the conductive wire W1 does not electrically connect with the first one of the at least two positive pads P or the at least two negative pads N (such as floating solder)), the manufacturer can make the same first end of the conductive wire W1 connect to another one of the at least two positive pads P or the at least two negative pads N without cleaning solder splash on the surface of the first one of the at least two positive pads P or the at least two negative pads N, thus the wire-bonding time (the wire-bonding efficiency) can be decreased and the wire-bonding yield can be increased.

[0043] In conclusion, the first surrounding colloid frame (such as a surrounding white colloid frame) of any shapes can be formed by coating in the instant disclosure. In addition, the position of the first package colloid body such as cured phosphor colloid can be limited in the first colloid position limiting space by using the first surrounding colloid frame, and the shape of the first package colloid body can be adjusted by using the first surrounding colloid frame. Therefore, the instant disclosure can increase the light-emitting efficiency of the light-emitting chips and control the light-projecting angle of the light-emitting chips. In other words, the first package colloid body is limited in the first colloid position limiting space by using the first surrounding colloid frame, thus the usage quantity of the first package colloid body can be controlled by the manufacture. In addition, the surface shape and the height of the first package colloid body can be adjusted by controlling the usage quantity of the first package colloid body, thus the light-projecting angles of the white light beams can be adjusted. Moreover, the blue light beams generated by the light-emitting chips can be reflected by an inner wall of the first surrounding colloid frame, thus the light-emitting efficiency of the instant disclosure can be effectively increased.

[0044] Moreover, the positive electrode and the negative electrode of each light-emitting chip respectively correspond to at least two of the positive pads and at least two of the negative pads, thus the positive electrode of each light-emitting chip has at least one standby positive pad and the negative electrode of each light-emitting chip has at least one standby negative pad.

[0045] Furthermore, the light-emitting chips and the at least one current-limiting chip are electrically connected to the same substrate body, thus the multichip package structure can use the constant voltage power supply as power supply source.

[0046] The above-mentioned descriptions merely represent the preferred embodiments of the instant disclosure, without any intention or ability to limit the scope of the instant disclosure which is fully described only within the following claims.

Claims

1. A multichip package structure (Z), comprising:

   a substrate unit (1) including a substrate body (10) having two first chip-placing regions (11) and a second chip-placing region (12) formed on the top surface of the substrate body (10);

   a light-emitting unit (2) including at least one first light-emitting module (2a) for generating first color temperature and at least one second light-emitting module (2b) for generating second

color temperature different from the first color temperature, wherein the first light-emitting module (2a) includes a plurality of first light-emitting chips (20a) electrically connected to and disposed on one of the first chip-placing regions (11), and the second light-emitting module (2b) includes a plurality of second light-emitting chips (20b) electrically connected to and disposed on the other first chip-placing region (11);

a current-limiting unit (C) including at least one current-limiting chip (C1) electrically connected to and disposed on the second chip-placing region (12), wherein the current-limiting chip (C1) is electrically connected to the light-emitting unit (2);

a frame unit (3) including two first surrounding colloid frames (30a, 30b) and a second surrounding colloid frame (31) surroundingly formed on the top surface of the substrate body (10) ; and

a package unit (4) including two distinct first package colloid bodies (40a, 40b) and a second package colloid body (41) wherein one (30b) of the first surrounding colloid frames (30a, 30b) surrounds the other first surrounding colloid frame (30a), the two first surrounding colloid frames (30a, 30b) respectively surround the first light-emitting module (2a) and the second light-emitting module (2b) to respectively form two first colloid position limiting spaces (300) corresponding to the two first chip-placing regions (11), the second light-emitting module (2b) is disposed between the two first surrounding colloid frames (30a, 30b), wherein the plurality of second light emitting chips (20b) surround the first light emitting module (2a), and the second surrounding colloid frame (31) surrounds the current-limiting chip (C1) to form a second colloid position limiting space (310) corresponding to the second chip-placing region (12), wherein the two first package colloid bodies (40a, 40b) are respectively filled into the two first colloid position limiting spaces (300) to respectively cover the first light-emitting module (2a) and the second light-emitting module (2b), and the second package colloid body (41) is filled into the second colloid position limiting space (310) to enclose the current-limiting chip (C1), wherein the two first surrounding colloid frames (30a, 30b) and the two first package colloid bodies (40a, 40b) are alternatively connected with each other.

2. The multichip package structure (Z) of claim 1, wherein the substrate body (10) includes a circuit substrate (100), a heat-dissipating layer (101) disposed on the bottom surface of the circuit substrate (100), a plurality conductive pads (102) disposed on the top surface of the circuit substrate (100), and an insulative layer (103) disposed on the top surface of the circuit substrate (100) to expose the conductive pads (102), wherein each light-emitting chip (20) is a blue LED, the first package colloid body (40) is a cured phosphor colloid or a cured transparent colloid, and the second package colloid body (41) is a cured opaque colloid.

3. The multichip package structure (Z) of claim 1, wherein the substrate unit (1) includes a plurality of positive pads (P) and negative pads (N) disposed on the top surface of the substrate body (10), each light-emitting chip (20) has a positive electrode (201) and a negative electrode (202), the positive electrode (201) of each light-emitting chip (20) corresponds to at least two of the positive pads (P), and the negative electrode (202) of each light-emitting chip (20) corresponds to at least two of the negative pads (N).

4. The multichip package structure (Z) of claim 3, further comprising: a conductive wire unit (W) including a plurality of conductive wires (W1), wherein every two conductive wires (W1) are respectively electrically connected between the positive electrode (201) of each light-emitting chip (20) and one of the at least two positive pads (P) and between the negative electrode (202) of each light-emitting chip (20) and one of the at least two negative pads (N).

5. The multichip package structure (Z) of claim 1, wherein the substrate unit (1) includes at least one heat-insulating slot (13) passing through the substrate body (10), and the heat-insulating slot (13) is formed between the light-emitting unit (2) and the current-limiting unit (C) or between the first surrounding colloid frame (30a) and the second surrounding colloid frame (31).

6. The multichip package structure (Z) of claim 1, further comprising a control unit (5) including at least one PWM control module (50) electrically connected to the at least one current-limiting chip (C1), wherein the current-limiting unit (C) is electrically connected between the control unit (5) and the light-emitting unit (2).

Patentansprüche

1. Multichip-Paketstruktur (Z), umfassend:

eine Substrateinheit (1) mit einem Substratkörper (10) mit zwei ersten Chip-Platzierbereichen (11) und einem auf der Oberfläche des Substratkörpers (10) ausgebildeten zweiten Chip-Platzierbereich (12),

eine lichtemittierende Einheit (2) mit zumindest

einem ersten lichtemittierenden Modul (2a) zur Erzeugung einer ersten Farbtemperatur und zumindest einem zweiten lichtemittierenden Modul (2b) zur Erzeugung einer von der ersten Farbtemperatur unterschiedlichen zweiten Farbtemperatur, wobei das erste lichtemittierende Modul (2a) eine Mehrzahl von ersten lichtemittierenden Chips (20a) aufweist, die mit einem der ersten Chip-Platzierbereichen (11) elektrisch verbunden und darauf angeordnet sind und das zweite lichtemittierende Modul (2b) eine Mehrzahl von zweiten lichtemittierenden Chips (20b) umfasst, die mit dem anderen ersten Chip-Platzierbereich (11) elektrisch verbunden und auf diesem angeordnet sind,
eine Strombegrenzungseinheit (C) mit zumindest einem mit dem zweiten Chip-Platzierbereich (12) elektrisch verbundenen und angeordneten Strombegrenzungs-Chip (C1), wobei der Strombegrenzungs-Chip (C1) mit der lichtemittierende Einheit (2) elektrisch verbunden ist,
eine Rahmeneinheit (3) mit zwei ersten umlaufenden Kolloidrahmen (30a, 30b) und einem zweiten umlaufenden Kolloidrahmen (31), der umgebend auf der Oberfläche des Substratkörpers (10) ausgebildet ist, und
eine Paketeinheit (4) mit zwei unterschiedlichen ersten Paketkolloidkörpern (40a, 40b) und einem zweiten Paketkolloidkörper (41),
wobei einer (30b) der ersten umlaufenden Kolloidrahmen (30a, 30b) den anderen ersten umlaufenden Kolloidrahmen (30a) umgibt, die zwei ersten umlaufenden Kolloidrahmen (30a, 30b) jeweils das erste lichtemittierende Modul (2a) und das zweite lichtemittierende Modul (2b) umgeben, um jeweils zwei erste Kolloidpositionsbegrenzungsräume (300) entsprechend den zwei ersten Chip-Platzierbereichen (11) auszubilden, wobei das zweite lichtemittierende Modul (2b) zwischen den beiden ersten umlaufenden Kolloidrahmen (30a, 30b) angeordnet ist,
wobei die Mehrzahl von zweiten lichtemittierenden Chips (20b) das erste lichtemittierende Modul (2a) und der zweite umlaufende Kolloidrahmen (31) den Strombegrenzungs-Chip (C1) umgibt, um einen dem zweiten Chip-Platzierbereich (12) entsprechenden zweiten Kolloidpositionsbegrenzungsraum (310) auszubilden, wobei die zwei ersten Paketkolloidkörper (40a, 40b) jeweils in die beiden ersten Kolloidpositionsbegrenzungsräume (300) eingefüllt werden, um das erste lichtemittierende Modul (2a) und das zweite lichtemittierende Modul (2b) jeweils abzudecken und der zweite Paketkolloidkörper (41) in den zweiten Kolloidpositionsbegrenzungsraum (310) gefüllt ist, um den Strombegrenzungs-Chip (C1) zu umschließen, wobei die beiden ersten umlaufenden Kolloidrahmen (30a, 30b) und die beiden ersten Paketkolloidkörpern (40a, 40b) abwechselnd miteinander verbunden sind.

2. Multichip-Paketstruktur (Z) nach Anspruch 1, wobei der Substratkörper (10) ein Schaltkreissubstrat (100), eine auf der Bodenfläche des Schaltkreissubstrats (100) angeordnete Wärmedissipationsschicht (101) eine Mehrzahl an auf der Oberfläche des Schaltungssubstrats (100) angeordneten leitfähigen Pads (102) und eine auf der Oberfläche des Schaltungssubstrats (100) angeordnete isolierende Schicht (103) aufweist, damit die leitfähigen Pads (102) freiliegen, wobei jeder lichtemittierenden Chip (20) ein blaues LED ist, der erste Packungskolloidkörper (40) ein gehärtetes Phosphorkolloid oder ein gehärtetes transparentes Kolloid ist und der zweite Packungskolloidkörper (41) ein gehärtetes opakes Kolloid ist.

3. Multichip-Paketstruktur (Z) nach Anspruch 1, wobei die Substrateinheit (1) mehrere auf der Oberfläche des Substratkörpers (10) angeordnete positive Pads (P) und negative Pads (N) aufweist, jeder lichtemittierende Chip (20) eine positive Elektrode (201) und eine negative Elektrode (202) aufweist, wobei die positive Elektrode (201) jedes lichtemittierenden Chips (20) zumindest zwei der positiven Pads (P) entspricht und die negative Elektrode (202) jedes lichtemittierenden Chips (20) zumindest zwei der negativen Pads (N) entspricht.

4. Multichip-Paketstruktur (Z) nach Anspruch 3, ferner umfassend: eine leitfähige Drahteinheit (W) mit mehreren leitfähigen Drähten (W1), wobei jeweils zwei leitfähige Drähte (W1) jeweils zwischen der positiven Elektrode (201) jedes lichtemittierenden Chips (20) und einem der zumindest zwei positiven Pads (P) und zwischen der negativen Elektrode (202) jedes lichtemittierenden Chips (20) und einer der zumindest zwei negativen Pads (N) elektrisch verbunden sind.

5. Multichip-Paketstruktur (Z) nach Anspruch 1, wobei die Substrateinheit (1) zumindest einen durch den Substratkörper (10) hindurchgehenden Wärmeisolierschlitz (13) aufweist und der Wärmeisolierschlitz (13) zwischen der lichtemittierenden Einheit (2) und der Strombegrenzungseinheit (C) oder zwischen dem ersten umlaufenden Kolloidrahmen (30a) und dem zweiten umlaufenden Kolloidrahmen (31) ausgebildet ist.

6. Multichip-Paketstruktur (Z) nach Anspruch 1, ferner umfassend eine Steuereinheit (5) umfasst, die zumindest ein mit dem zumindest einen Strombegrenzungs-Chip (C1) elektrisch verbundenes PWM-Steuermodul (50) umfasst, wobei die Strombegren-

zungseinheit (C) zwischen der Steuereinheit (5) und der lichtemittierenden Einheit (2) elektrisch verbunden ist.

Revendications

1. Structure de boîtier à plusieurs puces (Z), comprenant :

une unité substrat (1) qui comprend un corps de substrat (10) qui présente deux premières régions de placement de puce (11), et une seconde région de placement de puce (12) formée sur la surface supérieure du corps de substrat (10) ;
une unité électroluminescente (2) qui comprend au moins un premier module électroluminescent (2a) destiné à générer une première température de couleur, et au moins un second module électroluminescent (2b) destiné à générer une seconde température de couleur différente de la première température de couleur ;
dans laquelle le premier module électroluminescent (2a) comprend une pluralité de premières puces électroluminescentes (20a) connectées de manière électrique à l'une des premières régions de placement de puce (11), et disposées sur celle-ci, et le second module électroluminescent (2b) comprend une pluralité de secondes puces électroluminescentes (20b) connectées de manière électrique à l'autre première région de placement de puce (11) ;
une unité de limitation du courant (C) qui comprend au moins une puce de limitation du courant (C1) connectée de manière électrique à la seconde région de placement de puce (12), et disposée sur celle-ci, dans laquelle la puce de limitation du courant (C1) est connectée de manière électrique à l'unité électroluminescente (2) ;
une unité cadre (3) qui comprend deux premiers cadres colloïdaux environnants (30a, 30b) et un second cadre colloïdal environnant (31) formés de manière environnante sur la surface supérieure du corps de substrat (10) ; et
une unité boîtier (4) qui comprend deux premiers corps colloïdaux de boîtier distincts (40a, 40b) et un second corps colloïdal de boîtier (41) ;
dans laquelle l'un (30b) des premiers cadres colloïdaux environnants (30a, 30b) entoure l'autre premier cadre colloïdal environnant (30a), les deux premiers cadres colloïdaux environnants (30a, 30b) entourent respectivement le premier module électroluminescent (2a) et le second module électroluminescent (2b) de façon à former respectivement deux premiers espaces de limitation de la position colloïdale (300) qui correspondent aux deux premières régions de placement de puce (11), le second module électroluminescent (2b) est disposé entre les deux premiers cadres colloïdaux environnants (30a, 30b) ;
dans laquelle la pluralité de secondes puces électroluminescentes (20b) entourent le premier module électroluminescent (2a), et le second cadre colloïdal environnant (31) entoure la puce de limitation du courant (C1) de façon à former un second espace de limitation de la position colloïdale (310) qui correspond à la seconde région de placement de puce (12), dans laquelle les deux premiers corps colloïdaux de boîtier (40a, 40b) sont respectivement placés dans les deux premiers espaces de limitation de la position colloïdale (300) de façon à couvrir respectivement le premier module électroluminescent (2a) et le second module électroluminescent (2b), et le second corps colloïdal de boîtier (41) est placé dans le second espace de limitation de la position colloïdale (310) de façon à enfermer la puce de limitation du courant (C1), dans laquelle les deux premiers cadres colloïdaux environnants (30a, 30b) et les deux premiers corps colloïdaux de boîtier (40a, 40b) sont connectés de manière alternée les uns aux autres.

2. Structure de boîtier à plusieurs puces (Z) selon la revendication 1, dans laquelle le corps de substrat (10) comprend un substrat de circuit (100), une couche de dissipation de la chaleur (101) disposée sur la surface inférieure du substrat de circuit (100), une pluralité de plages conductrices (102) disposées sur la surface supérieure du substrat de circuit (100), et une couche isolante (103) disposée sur la surface supérieure du substrat de circuit (100) de façon à exposer les plages conductrices (102), dans laquelle chaque puce électroluminescente (20) est une LED bleue, le premier corps colloïdal de boîtier (40) est du phosphore colloïdal durci ou un colloïde transparent durci, et le second corps colloïdal de boîtier (41) est un colloïde opaque durci.

3. Structure de boîtier à plusieurs puces (Z) selon la revendication 1, dans laquelle l'unité substrat (1) comprend une pluralité de plages positives (P) et de plages négatives (N) disposées sur la surface supérieure du corps de substrat (10), chaque puce électroluminescente (20) présente une électrode positive (201) et une électrode négative (202), l'électrode positive (201) de chaque puce électroluminescente (20) correspond à deux au moins des plages positives (P), et l'électrode négative (202) de chaque puce électroluminescente (20) correspond à deux au moins des plages négatives (N).

4. Structure de boîtier à plusieurs puces (Z) selon la

revendication 3, comprenant en outre : une unité fil conducteur (W) qui comprend une pluralité de fils conducteurs (W1), dans laquelle les fils conducteurs (W1) sont respectivement connectés de manière électrique deux à deux entre l'électrode positive (201) de chaque puce électroluminescente (20) et l'une des deux plages positives (P) au moins, et entre l'électrode négative (202) de chaque puce électroluminescente (20) et l'une des deux plages négatives (N) au moins.

5. Structure de boîtier à plusieurs puces (Z) selon la revendication 1, dans laquelle l'unité substrat (1) comprend au moins une fente d'isolation thermique (13) qui passe à travers le corps de substrat (10), et la fente d'isolation thermique (13) est formée entre l'unité électroluminescente (2) et l'unité de limitation du courant (C), ou entre le premier cadre colloïdal environnant (30a) et le second cadre colloïdal environnant (31).

6. Structure de boîtier à plusieurs puces (Z) selon la revendication 1, comprenant en outre une unité de commande (5) qui comprend au moins un module de commande PWM (50) connecté de manière électrique à la ou aux puces de limitation du courant (C1), dans laquelle l'unité de limitation du courant (C) est connectée de manière électrique entre l'unité de commande (5) et l'unité électroluminescente (2).

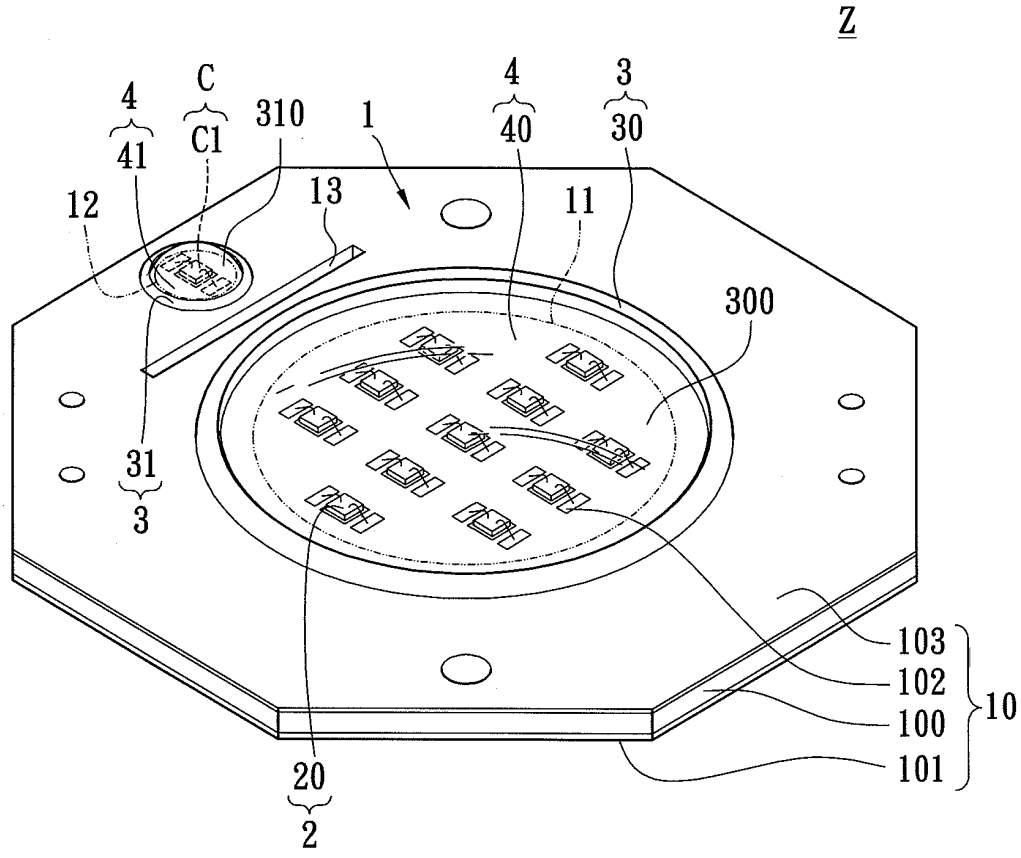
Z
4
41
C
C1
310
1
4
40
3
30
12
13
11
300
31
3
103
102
100
10
101
20
2

FIG. 1A

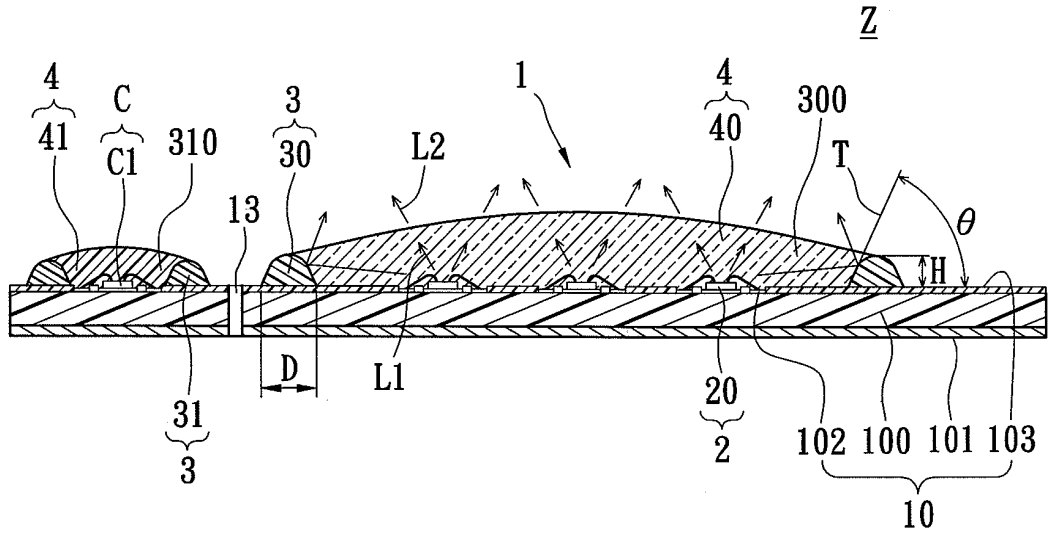
Z
4
41
C
C1
310
3
30
L2
1
4
40
300
T
θ
13
H
D
L1
31
3
20
2
102 100 101 103
10

FIG. 1B

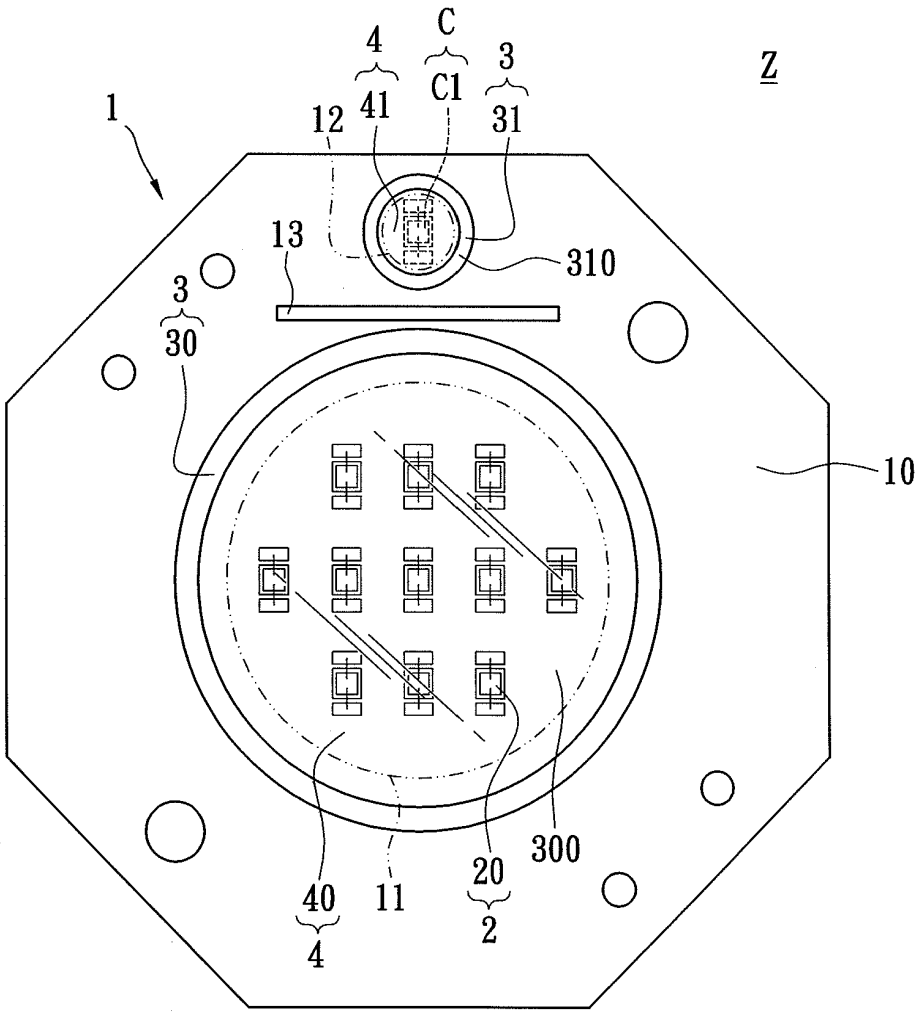
4
C
3
Z
1
12
41
C1
31
13
310
3
30
10
300
20
40
11
2
4

FIG. 1C

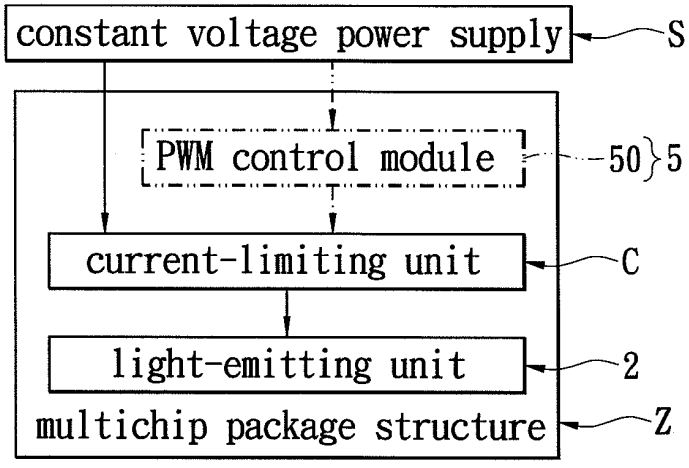
constant voltage power supply
S
PWM control module
50
5
current-limiting unit
C
light-emitting unit
2
multichip package structure
Z

FIG. 1D

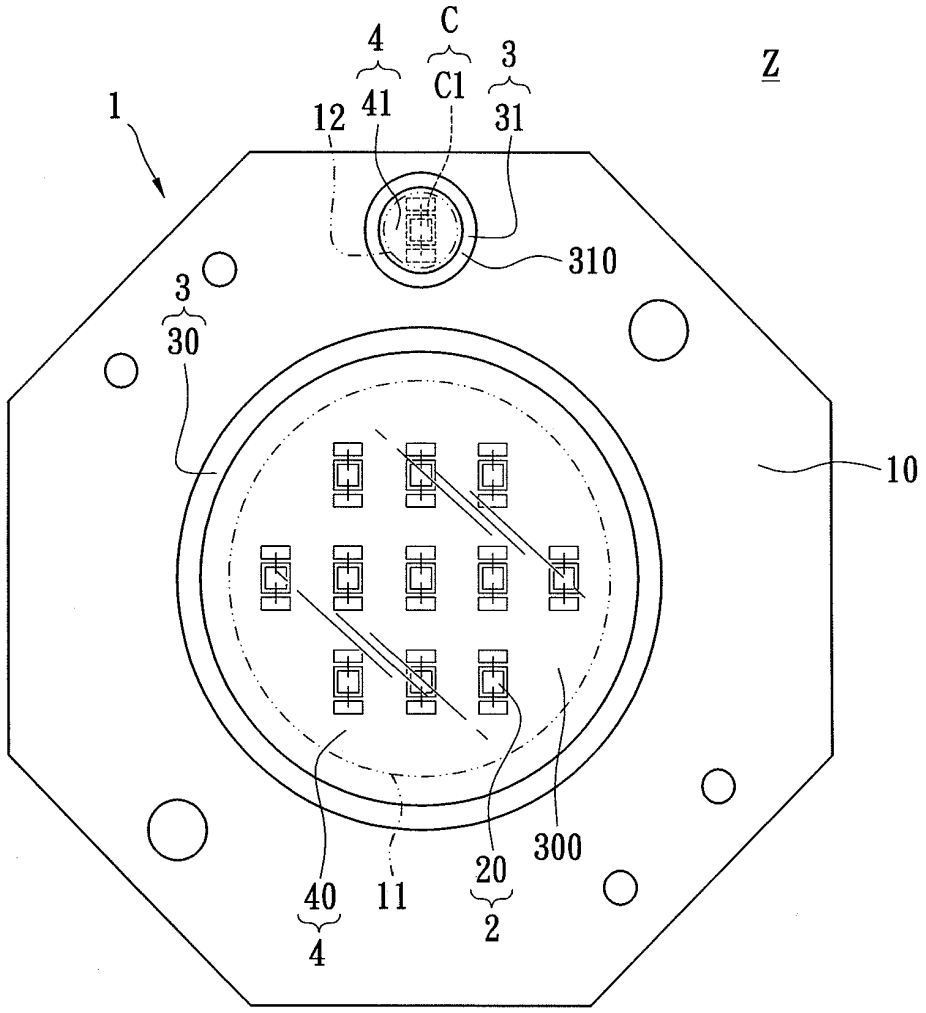
Z
1
4
41
C
C1
3
31
12
310
3
30
10
40
4
11
20
2
300

FIG. 2A

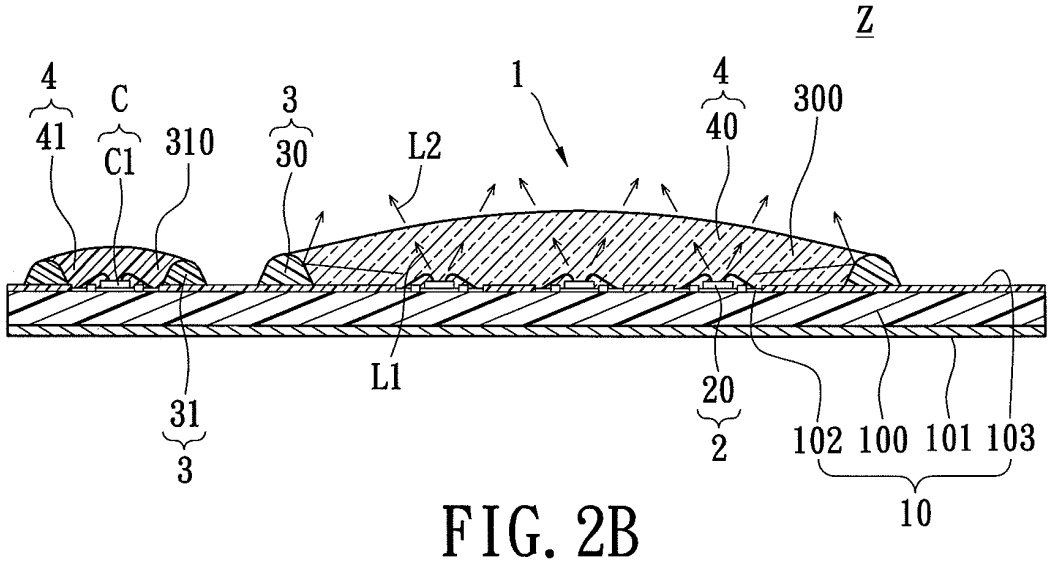
Z
4
41
C
C1
310
3
30
L2
1
4
40
300
L1
31
3
20
2
102
100
101
103
10

FIG. 2B

Z

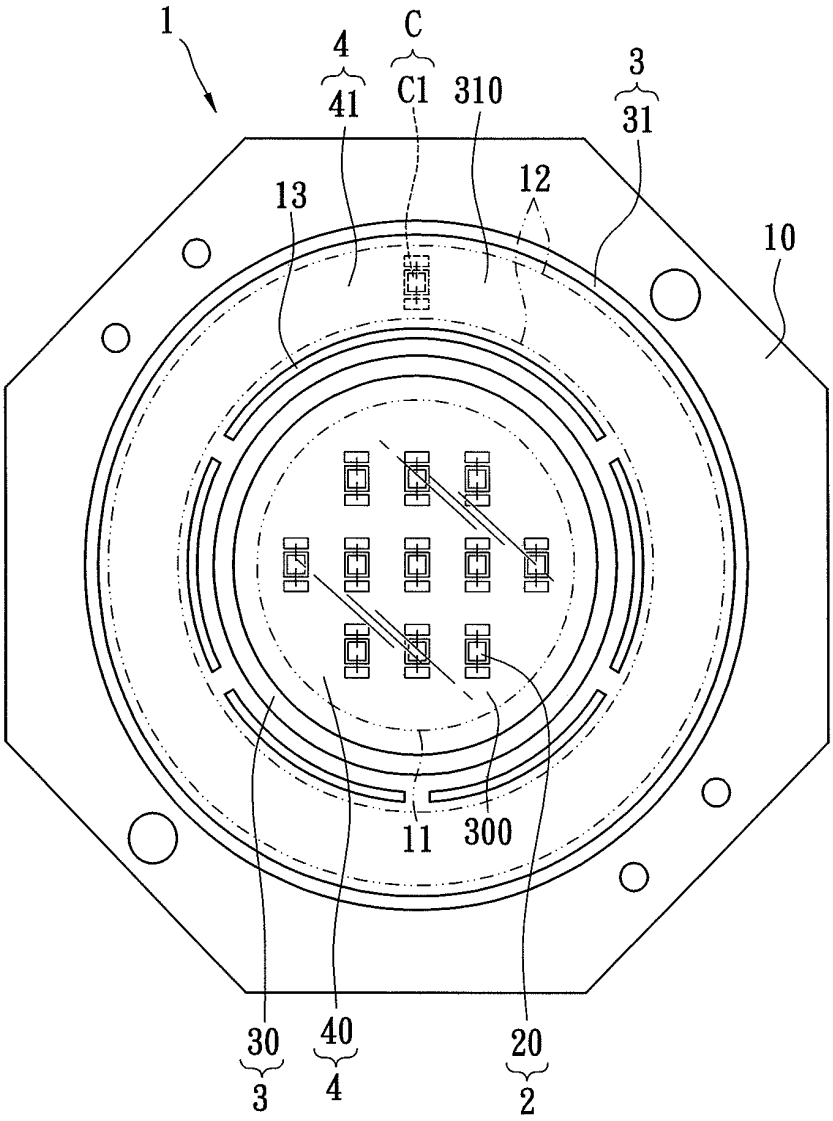

FIG. 3

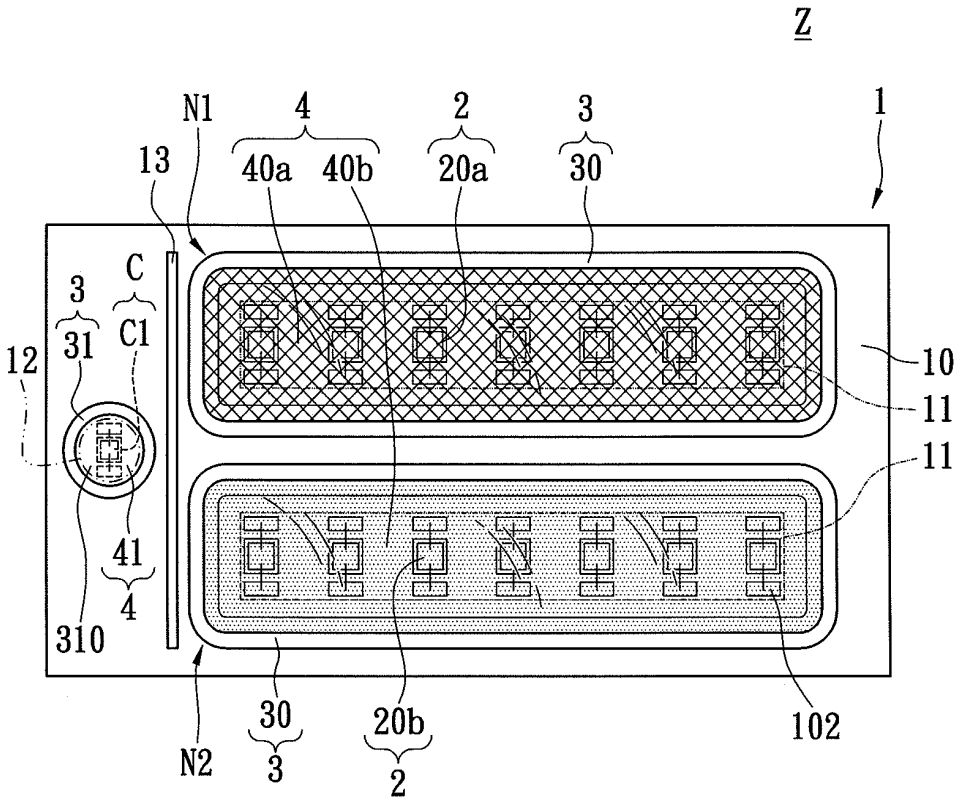
Z
N1
4
2
3
1
13
40a
40b
20a
30
3
C
31
C1
12
10
11
11
41
4
310
30
3
N2
20b
2
102

FIG. 4A

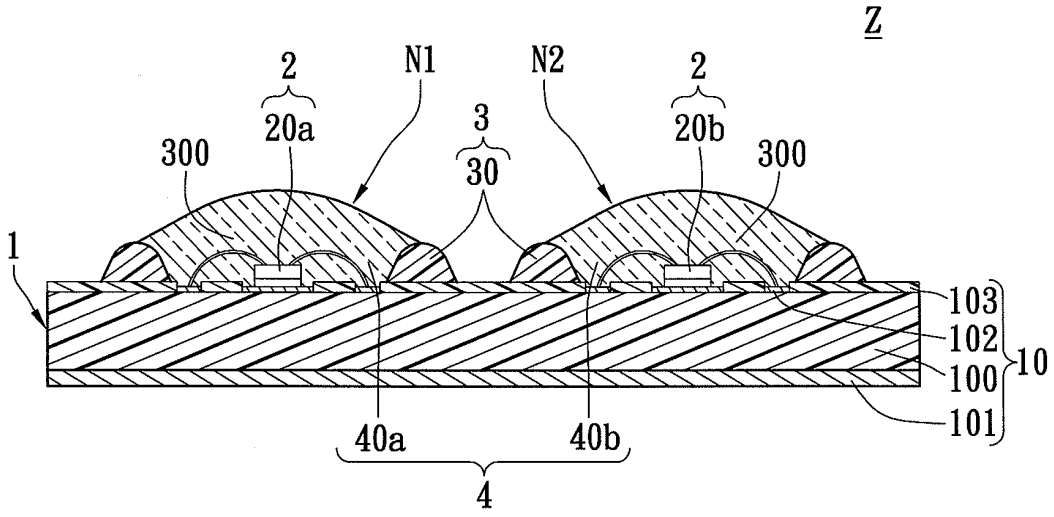
Z
2
N1
N2
2
20a
3
20b
300
30
300
1
103
102
10
100
101
40a
40b
4

FIG. 4B

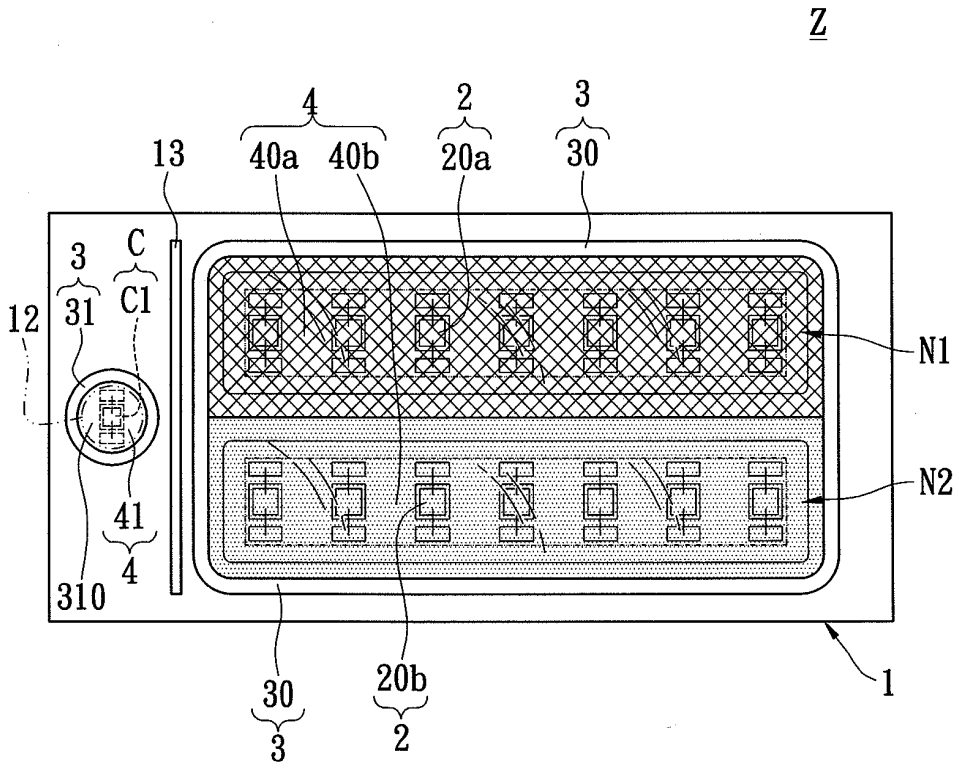
Z
4
2
3
13
40a
40b
20a
30
3
C
31
C1
12
N1
N2
41
4
310
30
3
20b
2
1

FIG. 5A

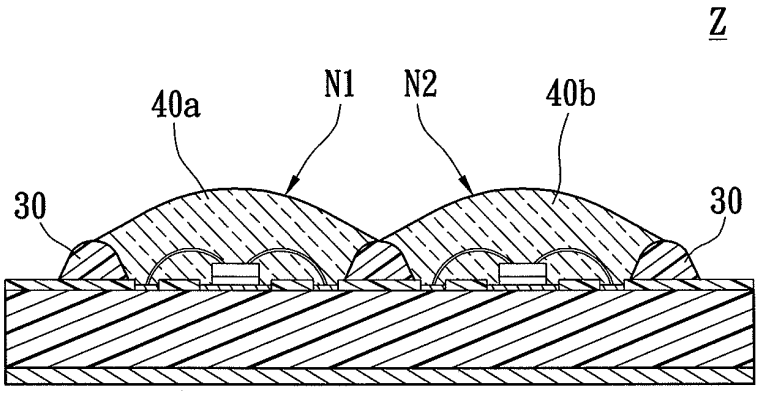
Z
40a
N1
N2
40b
30
30

FIG. 5B

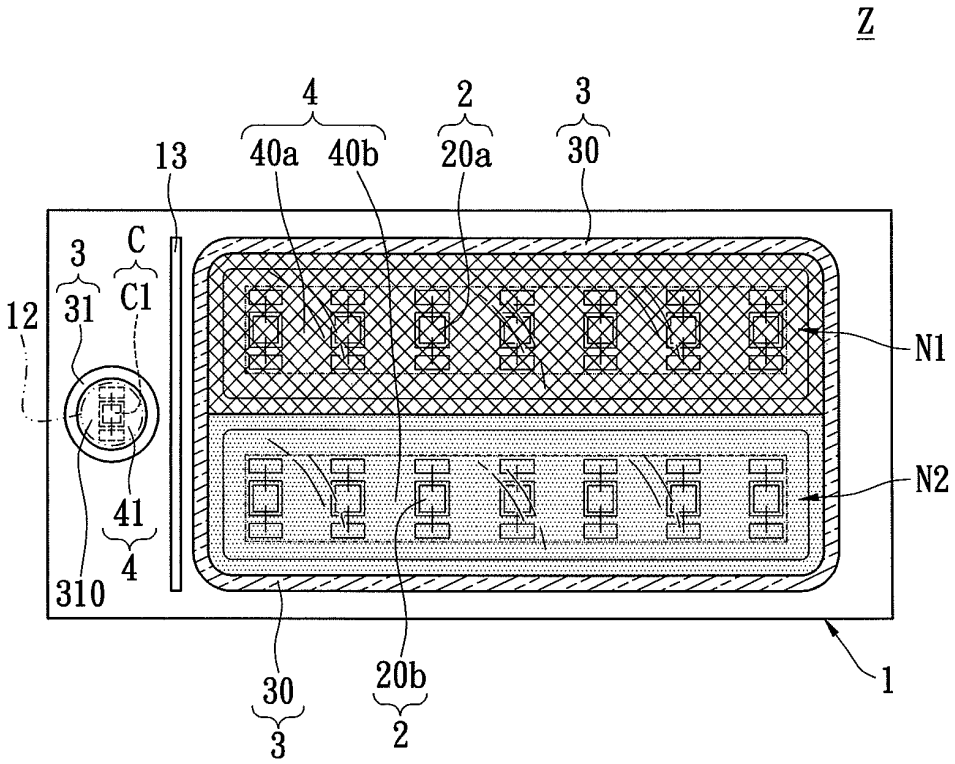
Z
4
2
3
13
40a
40b
20a
30
3
C
12
31
C1
N1
N2
41
4
310
30
3
20b
2
1

FIG. 6A

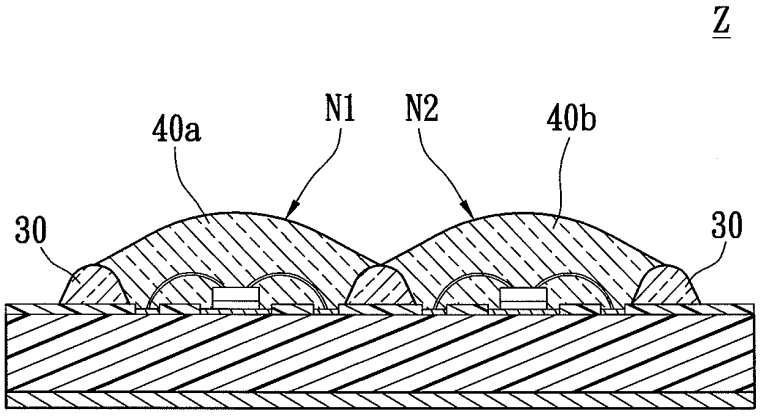
Z
N1
N2
40a
40b
30
30

FIG. 6B

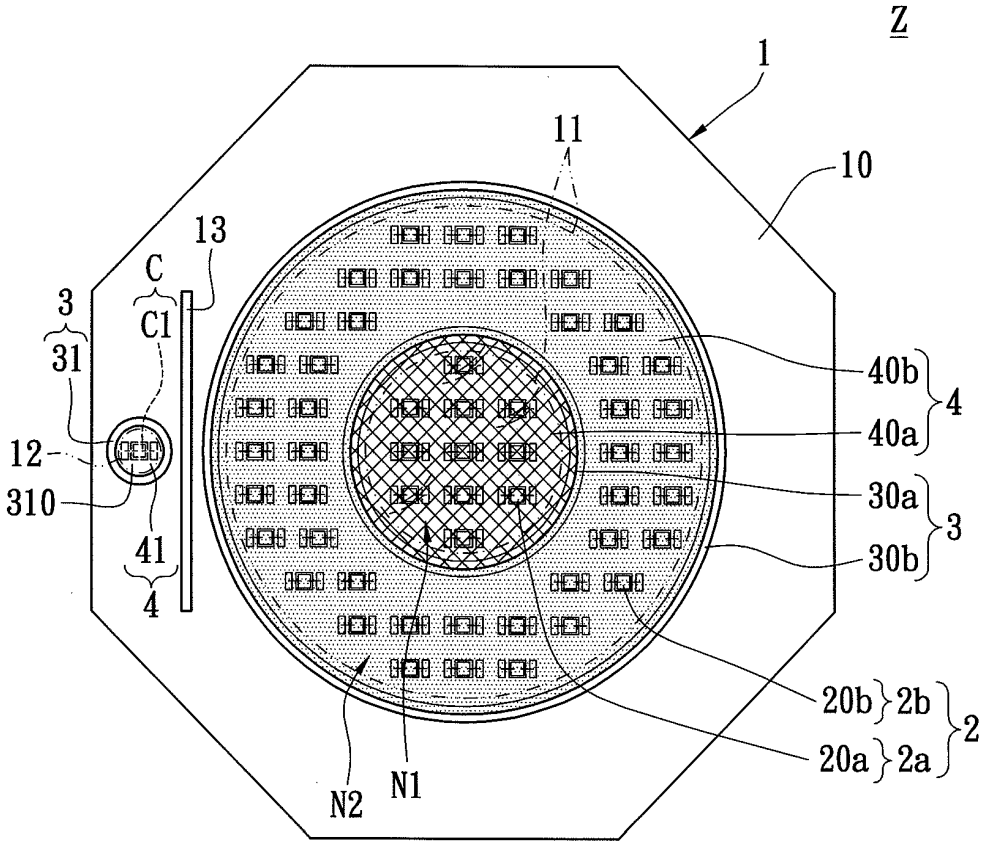
Z
1
11
10
13
C
C1
3
31
12
310
41
4
40b
40a
4
30a
30b
3
20b
2b
20a
2a
2
N2
N1

FIG. 7A

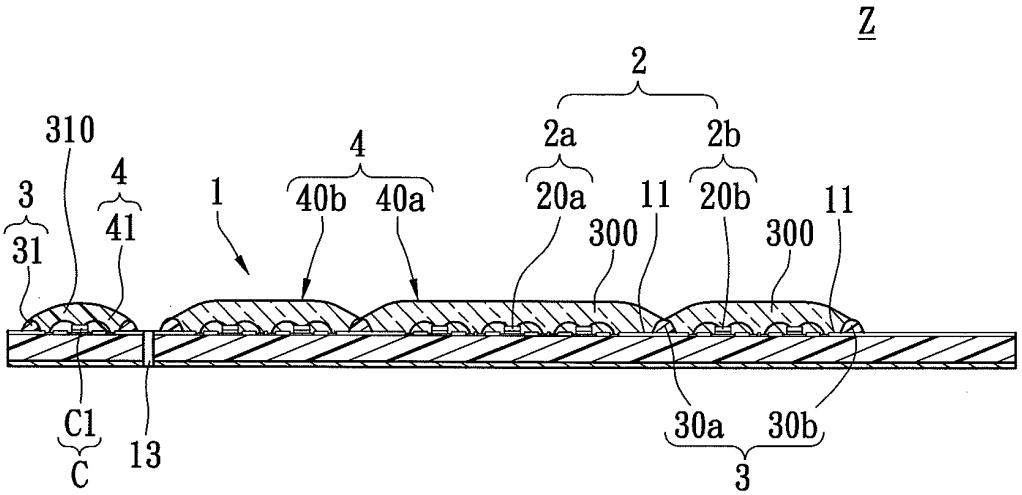
Z
2
2a
2b
310
4
3
41
31
1
40b
40a
20a
11
20b
11
300
300
C1
C
13
30a
30b
3

FIG. 7B

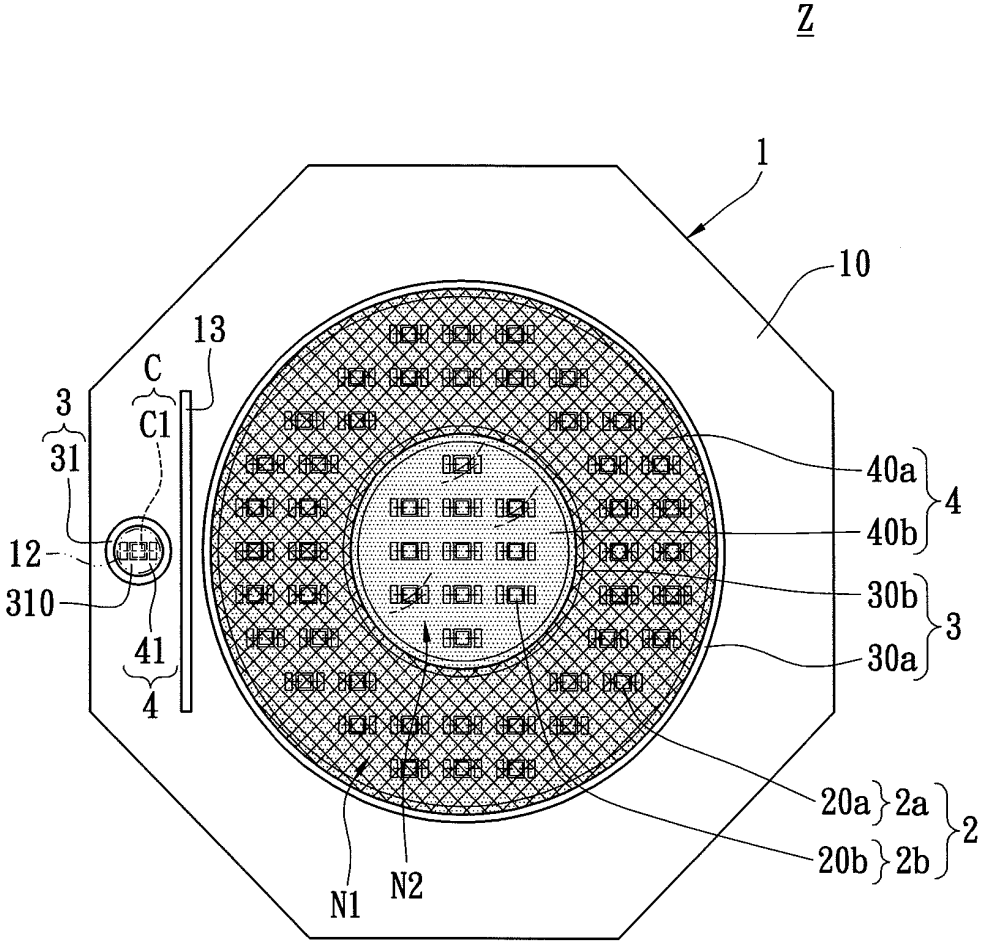

FIG. 8

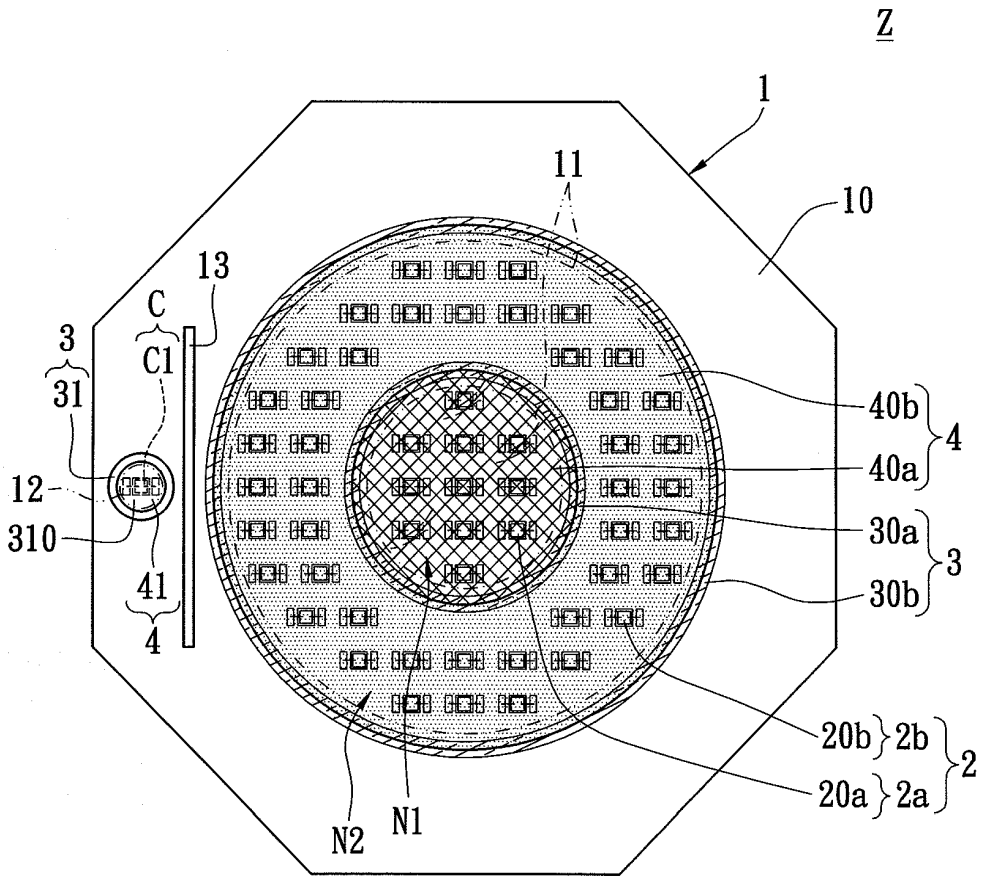
Z
1
11
10
13
C
C1
3
31
12
310
41
4
40b
40a
4
30a
30b
3
20b
2b
20a
2a
2
N2
N1

FIG. 9A

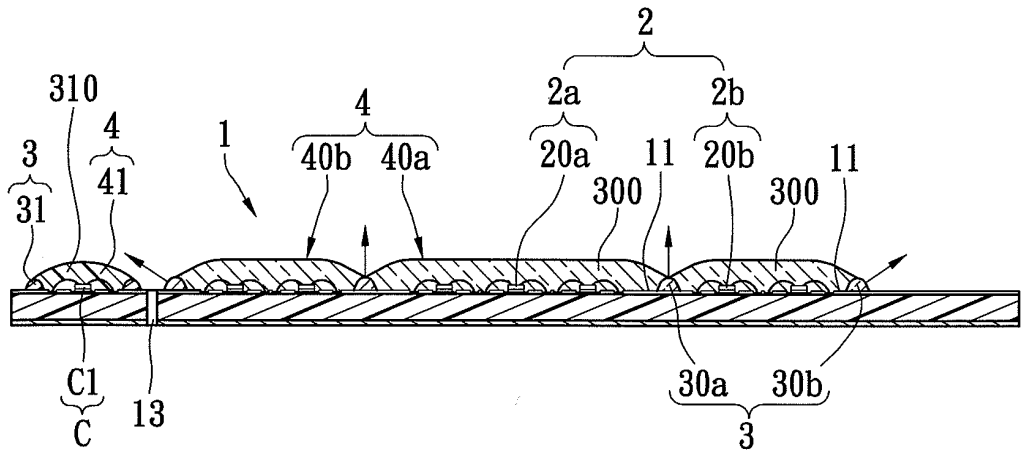
2
2a
2b
310
4
3
31
41
1
4
40b
40a
20a
11
20b
300
300
11
C1
C
13
30a
30b
3

FIG. 9B

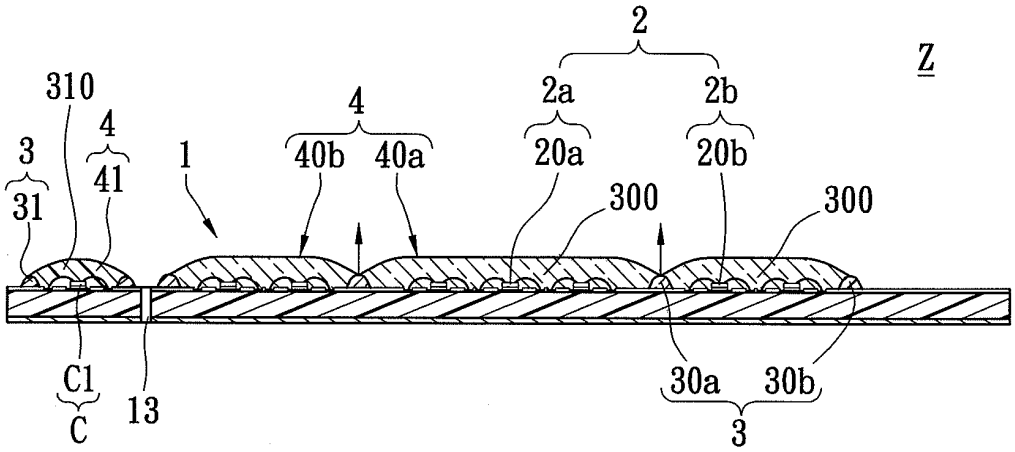
2
Z
310
4
2a
2b
3
4
40b
40a
1
20a
20b
41
300
300
31
C1
13
30a
30b
C
3

FIG. 10

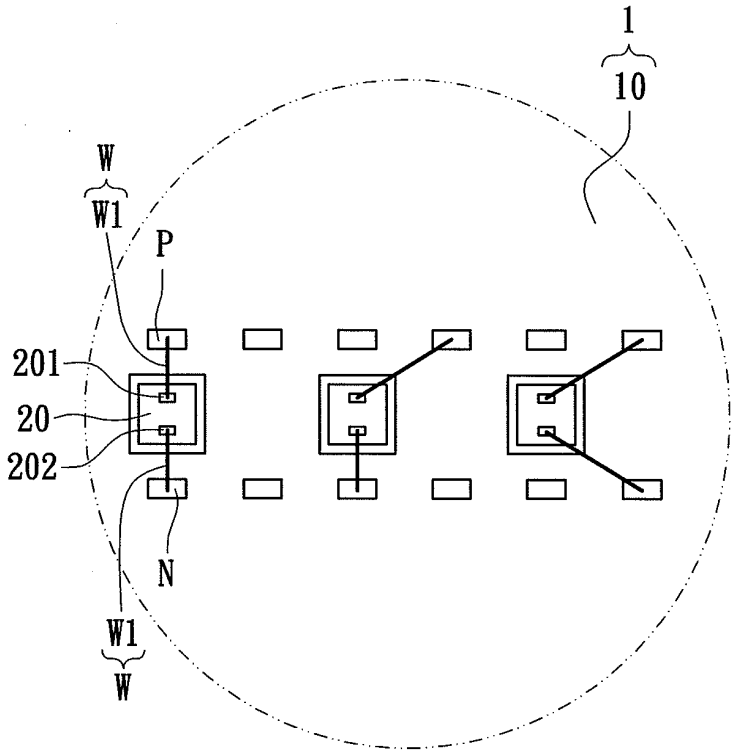
1
10
W
W1
P
201
20
202
N
W1
W

FIG. 11

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 06077540 B **[0002]**
- JP 2009117080 B **[0003]**
- WO 2008002073 A **[0004]**
- JP 2009231027 B **[0005]**